Zachodniopomorski Uniwersytet Technologiczny
w Szczecinie

Wydział Informatyki

21st Conference

RECONFIGURABLE UBIQUITOUS COMPUTING

RUC'2018

Szczecin – Dziwnów, October 12th, 2018

FRIDAY, 12th October, 2018

10:00 – 10:15 Conference Opening

10:15 – 11:45 SECTION: Applications

Chairman: Piotr Dziurzański

1. *Piotr Rzeszut, Ernest Jamro*
   AGH University of Science And Technology
   Oscilloscope based on small-size FPGA with VGA display
2. *Adam Klimowicz, Michał Sieniawski, Teodora Dimitrova-Grekow*
   Bialystok University of Technology
   Low cost Monitoring System of a Sitting Posture
3. *Jakub Tyburski*
   Military University of Technology
   Jumping-Jack – implementation of the game in programmable logic device
4. *Mieczysław Jessa, Jakub Nikonowicz*
   Poznan University of Technology
   Adaptation of the power spectral density of a pseudorandom Gaussian noise to the real radio-frequency noise of the ISM band
5. *Piotr Nikończuk, Sławomir Jaszczak*
   West Pomeranian University of Technology Szczecin
   A comparative analysis of temperature control algorithms for spray booths
6. *Grzegorz Ulacha, Cezary Wernik*
   West Pomeranian University of Technology Szczecin
   An implementation of Rice coder on AVR platform

11:45 – 12:15 Coffee Break

12:15 – 13:45 SECTION: Methods and Tools

Chairman: Aleksandr Cariow

1. *Adam Klimowicz*
   Bialystok University of Technology
   Speed Targeted Minimization of Finite State Machines for CPLDs
2. *Ryszard Szplet, Paweł Kwiatkowski, Krzysztof Różyc*
   Military University of Technology
   Digital-to-Time Converter for pulse train generation based on Look-Up Tables in FPGA
3. *Grzegorz Mazur*
   Warsaw University of Technology
   Event-driven firmware design with hardware handler scheduling on Cortex-M-based microcontroller
4. *Oleksander Chemerys, Sergii Sushko*
   Pukhov Institute for Modeling in Energy Engineering, NASU
   Dependency between Tiles' Sizes and Program Execution Time
5. *Valery Salauyou*
   Bialystok University of Technology
   Performance Targeted Synthesis of ASM Controllers on FPGA
6. *Jerzy Chrząszcz*
   Warsaw University of Technology
   TRIZ inventive principles and computer design

13:45 – 14:15 Coffee Break

14:15 – 15:45 SECTION: Hardware Acceleration

Chairman: Mirosław Łazoryszczak

1. *Kazimierz Wiatr, Bartłomiej Flak, Kamil Panek, Sebastian Koryciak*
   AGH University of Science And Technology
   Basic 3D graphics processor implemented on small FPGA
2. *Ryszard Szplet, Rafał Szymanowski, Dominik Sondej*
   Military University of Technology
   Evaluation of selected timing parameters of FPGA device
3. *Piotr Dziurzański*
   University of York
   Value-Based Smart Factories Optimisation and Reconfiguration in Serverless Clouds
4. *Aleksandr Cariow, Galina Cariowa*
   West Pomeranian University of Technology Szczecin
   Hardware-Efficient Structure of the Accelerating Module for Implementation of Convolutional Neural Network Basic Operation
5. *Tomasz Mąka, Piotr Dziurzański*
   West Pomeranian University of Technology Szczecin, University of York
   Mapping of hard real-time applications with unknown mode transition times to Network on Chips
6. *Aleksandr Cariow*
   West Pomeranian University of Technology Szczecin
   Basic Aspects of Designing a High-performance Processor Structure for Calculating a “true” Discrete Fractional Fourier Transform
7. *Krzysztof Arnold, Sławomir Michalak*
   Poznan University of Technology
   Programmable controller of microprocessoer ACE devices with SPI

18:00 – 22:00 Conference Dinner – Tawerna Żeglarska, ul. Mała 5, Dziwnów